

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Philip Mattos et al.
Application No. : 10/632,530
Filed : August 1, 2003
For : INTEGRATED CIRCUIT FOR CODE ACQUISITION
Examiner : Ted M. Wang
Art Unit : 2611
Docket No. : 851963.410
Date : March 28, 2007

Mail Stop Amendment
Assistant Commissioner for Patents
Washington, DC 20231

RULE 131 DECLARATION

Assistant Commissioner for Patents:

I, Ian Loveless, with a mailing address at Reddie & Grose, 16 Theobalds Road, London, WC1X 8PL, United Kingdom, declare as follows:

1. I am the UK patent attorney who filed European Patent Application No. 02255421.6 ("the EP application") on August 2, 2002, upon which the application identified above ("the present application") claims priority.

2. I received the disclosure of the invention prior to April 4, 2002. I diligently prepared the EP application, including the specification, claims, and figures and sent a first draft of the EP application to Mr. Mattos' attention prior to April 4, 2002 for his review, as evidenced by the attached transmittal letter (Exhibit 1). The date redacted in Exhibit 1 is prior to April 4, 2002.

3. I continued to further diligently prepare the EP application for filing, said diligence beginning at least as early as just before April 4, 2002, including my time spent preparing and revising the draft EP application (including working on a second draft on March 28,

2002). The completed second draft of the EP application was sent to Mr. Mattos' attention on April 5, 2002 for his review, as evidenced by the attached transmittal letter (Exhibit 2).

4. I continued to further diligently prepare the EP application for filing, up until the EP application was filed on August 2, 2002. These efforts included correspondence with Mr. Mattos on May 27, 2002, May 30, 2002, July 2, 2002, July 3, 2002, July 8, 2002, July 9 2002 and sending a revised draft application to Mr. Mattos' attention on July 25, 2002 (following a further meeting on July 11, 2002) for his review, as evidenced by the attached correspondence copies (Exhibits 3 to 7). The time gaps between these dates are at least partially attributable as a result of waiting for inventor review and inventor revision of the drafts. Waiting for a few weeks for comments from inventors is not unusual for the clients I have represented. Further, the time gaps between these dates are also at least partially attributable to my own patent attorney workload, where I have numerous on-going projects with various clients and their respective deadlines and my personal schedule. Thus, work on my projects (including the EP application) are allocated as my schedule and deadlines permit.

5. I, together with my staff, filed the EP application on August 2, 2002. My understanding is that the present application claims priority based on that European application.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

April 2, 2007
Date

Ian Loveless
Ian Loveless

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Philip.mattos@st.com
BY E-MAIL AND CONFIRMATION

IML/kz/43349/667

Dear Philip

Draft Patent Applications
Your Refs: ~~01-IMS-018~~
Our Files: 43349/50

I enclose by separate e-mail and also mail confirmation a first draft patent specification for two inventions, namely:

01-IMS-018

Using Adaptive Sampling Rate to Allow Faster GPS Acquisition Processing but More Accurate GPS Tracking Processing.

01-IMS-019

GPS Acquisition Acceleration Using a Circular Buffer Running Many Times Real-time Speed to Feed Samples to the Correlators.

I apologise for the delay in providing this draft to you. I had been instructed to delay filing the application, but then inadvertently have delayed drafting longer than usual. I have drafted a single document for the moment, and will divide this into two when preparing the final version.

On reviewing the materials you provided and my notes of our discussion, I think more information is required to meet the requirement that the invention is sufficiently described for someone to implement the invention on reading the description alone. In particular, this is in relation to the operation of the decimator, the two shift registers and the operation of either invention in the two modes (acquisition and tracking).

I have a series of meetings arranged with another inventor on Friday, 14 December 2001. If you are available, we could discuss the matter then, either to go through the matter in detail, or simply to discuss the further description and diagrams I think I need. Please let me know if this would be convenient - I think my earlier meetings should finish around 3 o'clock.

The questions I have are as follows:

01-IMS-018 (DECIMATOR)

The key to this invention appears to be the use of a decimator which reduces the number of samples of the received signal without losing information. From my notes, the way in which this is achieved is by some combinatorial logic, however, I cannot find in any of the materials the layout of that logic or a truth table. As this is the key to the invention, further description of this is required.

The decimator will convert the received CA code to a different sequence being a combination of the received sequence. Presumably, then, the locally generated code must be the same decimated combination of the original CA code.

How does the correlator work? In particular, there is a logic component numbered 32 which I assume represents logic such as an XOR gate arrangement. I need further description of this, and particularly how information is not lost when correlating the decimated signal.

The shift register shown in Figure 3, I assume, needs $1,023 \div 8$ locations for storage of the decimated CA code. What is not clear is what happens to the incoming data stream whilst the shift register is circulating at high speed. Is the incoming data simply lost?

Lastly, the circuit of Figure 3 must be able to operate in the two modes (acquisition and tracking) and yet the circuit, as shown, could only operate in the acquisition mode. I need some explanation of how the circuit can operate in tracking mode.

01-IMS-019 (TWO SHIFT REGISTERS)

The questions above in relation to the decimator apply equally to this invention. In particular, I note that the special case where the decimator, shift registers and number of channels mean that processing at $2,048 \times$ normal is achieved is mentioned. This means that all the incoming data can be captured and processed. I assume that without this special condition being met, data must simply be lost.

I believe the functionality of swapping from one shift register to another is adequately described. However, are there any special requirements of the size of the shift register?

I also need some description of how this invention, as shown in Figure 4, can swap between the two modes of acquisition and tracking. Are the shift registers involved at all in the tracking mode?

GENERAL COMMENTS

I have included Figures 5, 6 and 7 but not written any description in relation to these. Is the arrangement disclosed in these figures standard or is this a new feature? If it is standard, no description is required. If new, then we should describe this further.

Yours sincerely

Ian M Loveless
ian.loveless@reddie.co.uk

Enc
Apps2

Philip Mattos Esq.
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Philip.mattos@st.com
BY E-MAIL AND CONFIRMATION

5 April 2002
IML/kz/43349/50y

Dear Philip

Draft Patent Applications
Your Refs: ~~01-IMS2019/9~~
Our Files: 43349/50

I enclose by e-mail and mail confirmation a second draft patent specification in respect of these two inventions. I apologise for the delay in providing this to you; I had a period of paternity leave shortly after our meeting which delayed matters somewhat.

The draft is substantially revised from the first draft and so I have not attempted to produce a comparison of the two documents. As a guide, though, I have reordered the description so that the two shift register version is the main embodiment (where the single shift register is mentioned at the end for completeness). I have also incorporated some description of the possible decimator arrangements, which is central to the invention, which you provided at our meeting. I have also tried to include some of the alternative arrangements which you invented during the course of our meeting! I have also now produced a full claim set and would ask that you review these first. There are two claim sets, one in respect of each invention, which I have kept together for the moment though, ultimately, they will be filed as separate applications. Please review claim 1 of each claim set as this sets out the broadest protection we are seeking. You need to satisfy yourself that there are no trivial alternatives of the invention which would fall outside the scope of each of these claims. Similarly, please satisfy yourself that the claims are not so broad as to cover any known systems. In preparing the claims, it seems to me that the operation in acquisition and tracking modes is central to the inventions as, without any explanation of these two modes, the claims would arguably read on to other unrelated systems. I have selected various terms for the components and signals and would be grateful if you would consider these carefully as to whether they are correct.

If you feel that the description should be expanded or any further drawings should be included, please feel free to provide me with these. In particular, in our meeting I know that you were thinking of alternatives as we discussed the matter, and it may be that I have missed some of these which could be pertinent.

I look forward to hearing from you.

Yours sincerely

Ian M Loveless

ian.loveless@reddie.co.uk

Enc
Specs

To: philip.mattos@st.com
Subject: Patent Applications

Philip Mattos Esq.
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Philip.mattos@st.com
BY E-MAIL AND CONFIRMATION

27 May 2002
IML/kz/43349/50

Dear Philip

Draft Patent Applications
Your Refs: 01-IMS-018/9
Our Files: 43349/50

I refer to my e-mail of 5 April 2002. I recently met with Jean-Jacques de Jong and he asked after the status of these applications. Accordingly, I thought I would send a short e-mail as a reminder that I am waiting for your review.

Yours sincerely

Ian M Loveless
ian.loveless@redddie.co.uk

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This footnote also confirms that this email message has been swept by MIMESweeper for the presence of computer viruses.

Reddie & Grose
10 Theobalds Road
London, WC1X 8PL
United Kingdom

From: "Philip Mattos" <philip.mattos@st.com>
To: <Ian.Loveless@reddie.co.uk>
Date: 30/05/02 10:57
Subject: RE: Patent Applications

Do you mean July ??? I can do 11th all day, but only the morning on the 12th.

Sounds a bit late to get it filed before September conferences.

If you meant June.... I can do 11th and 12th at the moment.

Current state of documentation will be sent in next email... highly confidential therefore zipped with password "██████████" all in lower case.

Philip

-----Original Message-----

From: Ian.Loveless@reddie.co.uk [mailto:ian.Loveless@reddie.co.uk]
Sent: 27 May 2002 17:12
To: philip.mattos@st.com
Subject: RE: Patent Applications

Philip

I am trying to coordinate some meetings on 11th and 12th July. Are either of these any good to you? If you have some written material to send me in advance, that would certainly help.

Regards

Ian

>>> "Philip Mattos" <philip.mattos@st.com> 27/5/02 4:33:32 pm >>>
Hi,

Sorry for the delay/silence.... either one was ok but not both !!!

I did review the documents immediately, but I found that changes were going to be so drastic that we would need to meet again.

The main problem is that with a 2 month loop delay, I have redesigned the whole thing before the text is written !!!

So I decided to wait until the design stabilised at my end.

Anyway... now I have not only redesigned the whole thing but even documented it... with powerpoint block diagrams and even mathematical proofs of algorithms

If we can still get something filed before the end of August, then I would like to proceed at full speed.... when can we get together ???

Philip

-----Original Message-----

From: Ian.Loveless@reddie.co.uk [mailto:ian.Loveless@reddie.co.uk]
Sent: 27 May 2002 14:52

From: "Philip Mattos" <philip.mattos@st.com>
To: <Ian.Loveless@reddie.co.uk>
Date: 08/07/02 10:40
Subject: RE: Visit Friday 12 July

Yes, fine

See you then

Philip

-----Original Message-----

From: Ian.Loveless@reddie.co.uk [mailto:Ian.Loveless@reddie.co.uk]
Sent: 08 July 2002 10:15
To: philip.mattos@st.com
Subject: RE: Visit Friday 12 July

Philip

Could we say the morning around 10.30 a.m.?

Ian

>>> "Philip Mattos" <philip.mattos@st.com> 3/7/02 8:28:15 am >>>
Yes Thursday 11th is fine.

am or pm / time ??

Philip

-----Original Message-----

From: Ian.Loveless@reddie.co.uk [mailto:Ian.Loveless@reddie.co.uk]
Sent: 02 July 2002 14:50
To: philip.mattos@st.com
Subject: Visit Friday 12 July

Philip

I have your new diagrams and will do my best to incorporate changes for review before/ at our meeting next week.

Is it possible to swap the meeting, though, to Thursday 11th instead of Friday 12th? Another inventor at the Bristol site has a clash in their diary.

Thanks

Ian

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From: Ian Loveless
To: Philip Mattoe
Date: 9/7/02 5:18:58 pm
Subject: RE: Visit Friday 12 July

Philip

I have now worked through the new diagrams that you sent. I shall certainly need an explanation to fully understand the new proposal! I have not, therefore, attempted to work the new proposal into the existing draft application yet.

It strikes me that the new proposal uses the same basic techniques as already described in the draft application, namely some form of sample reduction and subsequent correlation at a faster than usual rate. We should perhaps explore at our meeting whether we should be filing one, two or three separate applications, or perhaps just one including all the ideas (with the aim of dividing the application later).

I look forward to our meeting.

Regards

Ian

From: Ian Loveless
To: Philip.mattos@st.com
Date: 25/7/02 5:37:29 pm
Subject: Draft Patent Applications Your Refs: 01-IMS-018/9

Philip Mattos Esq.
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Philip.mattos@st.com
BY E-MAIL AND CONFIRMATION

25 July 2002
IML/kz/43349/50EP

Dear Philip

Draft Patent Applications
Your Refs: 01-IMS-018/9
Our Files: 43349/50EP

Following our third meeting on 11 July 2002, I enclose with this e-mail two separate draft patent specifications and figures. The specifications are in word format, as requested, and I have zipped them using the same password as the password you used to send material to me. I am also copying this e-mail to Jean-Jacques de-Jong, as I feel a policy decision needs to be taken on how to proceed with this application or applications.

It appears to me that there may be three separate ideas in the various different embodiments you have described:

1. The use of the decimator, along with the existing channels used for tracking to increase acquisition speed.
2. The use of a memory arrangement (the two shift registers), along with the existing channels used for tracking to increase the speed of acquisition.
3. The use of a decimator which produces a parallel output to a separate correlator which is used for acquisition purposes only and not for tracking.

There are advantages to each solution, such as the first and second, reusing the existing correlators but still increasing speed and, with the third idea, the possible future use on the next generation of positioning signals.

I have, for the moment, kept the first and second ideas as one draft and this is basically the same as when it was last sent to you for review. I have drafted the third idea as a new application for the moment as it seems to me that this is a separate idea, as the use of a decimator which produces a parallel data output means that the existing correlators are not used but a separate acquisition engine is provided.

Firstly, could you consider the points discussed above and let me know if I have understood correctly. Are the first and second ideas viable options which you would like to prevent others from using?

Secondly, please review the new draft and let me have some further explanation. As requested, the

document is in word format, so that it may be simpler for you to add comments or text, as appropriate. I am happy that the description of the data streaming decimator and first part of the correlator are reasonably straight, but the second part of the first correlator, the frequency handling and the second integration are not entirely clear. Perhaps you could let me have a few words of explanation. I have drafted a single independent claim for the moment pending further information.

I had just finished drafting the application for the new invention when I received your e-mail of 24 July 2002 regarding the fact that you derive the 16 MHz clock from a local oscillator and you ask whether or not this should be a separate patent application. It appears that this is fundamentally a different idea (although it may be implemented on the same embodiment) from the previous ideas we have discussed, and so would need to be a separate patent application. However, is the idea of using one clock source for two different purposes in a GPS receiver really new? If I understand correctly, the invention is in using a single clock source for the radio section and the digital section. If this is new, then I would need a separate write-up and authority from Jean-Jacques de Jong to proceed. I am copying this e-mail to Jean-Jacques for instructions on that point.

I know that our deadline is the end of August, as you intend to disclose the invention then, now that you have finalised the idea. I am in the office all next week and can set aside time for a telephone discussion if this will help.

I look forward to hearing from you.

Yours sincerely

Ian M Loveless
ian.loveless@reddie.co.uk

Enc
Draft Specsx2, Figs

cc: Jean-Jacques de Jong Esq.,
jean-jacques.de-jong@st.com